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# Josephson phase qubit circuit for the evaluation of advanced tunnel barrier materials\*

Jeffrey S Kline,<sup>1</sup> Haohua Wang,<sup>2</sup> Seongshik Oh,<sup>1†</sup> John M Martinis<sup>2</sup> and David P Pappas<sup>1</sup>

<sup>1</sup>National Institute of Standards and Technology, Boulder, Colorado 80305, USA

<sup>2</sup>Department of Physics, University of California, Santa Barbara, California 93106, USA

<sup>†</sup>Present address: Department of Physics & Astronomy, Rutgers, The State University of New Jersey, Piscataway, NJ 08854

Electronic mail: klinej@nist.gov

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## Abstract

We have found that crystalline Josephson junctions have problems with control of critical current density that decrease circuit yield. We present a superconducting quantum bit circuit designed to accommodate a factor of five variation in critical current density from one fabrication run to the next. The new design enables the evaluation of advanced tunnel barrier materials for superconducting quantum bits. Using this circuit design, we compare the performance of Josephson phase qubits fabricated with MgO and Al<sub>2</sub>O<sub>3</sub> advanced crystalline tunnel barriers to AlO<sub>x</sub> amorphous tunnel barrier qubits.

## 1. Introduction

One of the greatest challenges in the development of a practical solid-state quantum computer is to overcome quantum decoherence due to unwanted coupling between the environment and the quantum bit (qubit) [1]. The performance of superconducting Josephson phase qubits is presently limited by decoherence due to microwave dielectric loss in both the tunnel barrier [2] and wiring crossover insulator [3]. Thus, the dominant sources of decoherence originate within the material components of the qubit itself. Dielectric loss in the tunnel barrier can be reduced by use of advanced tunnel barrier materials [4] or by reducing the area of a high-loss tunnel junction [5]. Likewise, dielectric loss in the wiring crossover insulators can be reduced by use of low-loss insulators [3,6] or by reducing the volume of a high-loss insulator.

Optimization of the materials used in the tunnel barrier can improve qubit performance. For example, measurement fidelity of the ground and excited states ( $|0\rangle$  and  $|1\rangle$ ) of the qubit and the energy relaxation time  $T_1$  improves as the number of spurious two-level states (TLS) in the tunnel barrier decreases. TLS are defect states with a non-zero electric dipole that dissipate energy in a resonant microwave electric field [7]. Oh *et al* demonstrated that the usage of a crystalline Al<sub>2</sub>O<sub>3</sub> tunnel barrier reduces the density of TLS by ~80% compared to the ubiquitous amorphous AlO<sub>x</sub> tunnel barrier [4]. This reduction in density of TLS can be explained by the higher coordination number and crystallinity of Al<sub>2</sub>O<sub>3</sub> compared to that of AlO<sub>x</sub>.

The investigation of advanced tunnel barrier materials for qubits can be hindered by variations in critical current density ( $J_c$ ) from one deposition run to the next. We find that low leakage Re/Al<sub>2</sub>O<sub>3</sub>/Al and Re/MgO/Al Josephson junctions with crystalline tunnel barriers, where the barrier is fabricated by reactive evaporation [8], have a greater variation in  $J_c$  than do amorphous tunnel barriers fabricated by thermal oxidation of Al. This variation in  $J_c$  could be caused by variations in the tunnel barrier thickness due to instability in the reactive evaporation rate, or by the relatively smaller number of “hot spots” [9] that are predicted for crystalline tunnel barriers [10]. Also, in the commonly used thermal oxidation technique for the fabrication of amorphous junctions, the thickness of the tunnel barrier depends logarithmically on deposition time and is relatively insensitive to small variations in oxidation time. In

contrast, the reactive evaporation method is linear in time and is more sensitive to variations in deposition time and evaporation rate.

The junction critical current ( $I_c$ ) is related to  $J_c$  via  $I_c = J_c A$ , where  $A$  is the junction area, and may vary from  $1 \mu\text{A}$  to  $5 \mu\text{A}$  for  $5 \mu\text{m} \times 5 \mu\text{m}$  junctions, from one deposition run to the next, where the tunnel barrier deposition conditions are the same for each run. This variation in  $I_c$  by a factor of five makes it difficult to fabricate a working qubit circuit that requires  $I_c$  in the range of  $1.1 \mu\text{A}$  to  $2.8 \mu\text{A}$ .

To circumvent the issues in control of critical current density associated with crystalline tunnel junctions and presumably other advanced tunnel junctions, we have designed a qubit circuit that can accommodate the above mentioned variation in junction critical current. This circuit design is useful for evaluating advanced tunnel barrier materials where the control of critical current density may not be as good as that for established tunnel barrier technologies.

## 2. Fabrication and Processing

We fabricated the qubit circuits on crystalline  $\text{Al}_2\text{O}_3(0001)$  substrates ( $12.7 \text{ mm} \times 15 \text{ mm} \times 0.43 \text{ mm}$ ) using an epitaxial trilayer process described in [8]. Briefly, the trilayer consists of a crystalline rhenium base electrode  $160 \text{ nm}$  thick, a crystalline  $\text{Al}_2\text{O}_3$  or  $\text{MgO}$  tunnel barrier  $\sim 1.5 \text{ nm}$  thick and a polycrystalline aluminum top electrode  $100 \text{ nm}$  thick. The base electrode is deposited at high substrate temperature ( $\sim 1100 \text{ K}$ ) by sputtering. The tunnel barrier is grown by reactive evaporation of Al or Mg in a molecular oxygen background ( $10^{-4} \text{ Pa}$ ) at room temperature. In addition, the  $\text{Al}_2\text{O}_3$  tunnel barrier requires a post-growth high-temperature anneal ( $\sim 1050 \text{ K}$ ) for crystallization. The top electrode is deposited by evaporation at room temperature.

We performed lateral trilayer patterning using optical lithography, ion milling and plasma- and wet-etching techniques. The wiring crossover insulator is amorphous  $\text{SiO}_2$   $360 \text{ nm}$  thick deposited by plasma enhanced chemical vapor deposition at room temperature. The volume of the high-loss  $\text{SiO}_2$  insulator [11] has been minimized by retaining it only where necessary for separation of wiring layers. This is accomplished use of a self-aligned reactive ion etch of  $\text{SiO}_2$  after the completion of the Al wiring ( $100 \text{ nm}$  thick, sputter deposited at room temperature) layer patterning.

## 3. Circuit Design

The individual qubit circuit is similar to the design described in [12]. It consists of a flux biased Josephson phase qubit with a Josephson junction in a gradiometer loop. An overlapped gradiometer three-junction direct current superconducting quantum interference device (SQUID) with  $64 \text{ pH}$  mutual inductance between the qubit and SQUID loop is used for qubit state readout measurement, as shown in figure 1. The three-junction SQUID design is used so that the SQUID-qubit coupling can be modulated. One branch of the SQUID loop has a single Josephson junction with critical current  $I_c = 1.6 \mu\text{A}$  and capacitance  $C \sim 2 \text{ pF}$ , and the other branch has two larger junctions each with critical current  $1.7 \times I_c$ . The qubit loop with inductance  $L = 722 \text{ pH}$  is sensitive to the flux bias coil through mutual inductance  $M = 2.67 \text{ pH}$ , but the SQUID loop has negligible mutual inductance, due to its symmetric position with respect to the gradiometric flux bias coil.

The qubit and SQUID Josephson junctions are square. The smallest linewidth and line spacing of wires is  $2 \mu\text{m}$  and  $1.5 \mu\text{m}$ , respectively. A perforated ground plane with  $10 \mu\text{m} \times 10 \mu\text{m}$  holes is used to immobilize trapped magnetic flux. The flux bias coil and qubit loop are fabricated primarily from base layer material (Re) and the SQUID loop is fabricated primarily from wiring layer material (Al). The usage of Re, which does not readily oxidize, for the qubit loop may reduce the  $1/f$  flux noise in the qubit [13] due to the reduced number of TLS in the native oxide of the superconductor [14].

The unintentional variation in critical current density of our crystalline Josephson junctions makes proper circuit operation a challenge. Many deposition systems equipped with in-situ surface characterization equipment suitable for advanced tunnel barrier growth and characterization can only accommodate small chip-sized ( $\sim 1 \text{ cm} \times 1 \text{ cm}$ ) substrates, as opposed to traditional deposition systems that may utilize wafers  $75 \text{ mm}$  in diameter or larger. To obtain the highest possible yield of qubit devices on a small  $12.5 \text{ mm} \times 15 \text{ mm}$  chip that contains only two dies, we placed twelve qubit circuits on each 6

mm  $\times$  6 mm die. This amounts to an increase of three times as many qubit circuits compared to a previous crystalline qubit study [4].

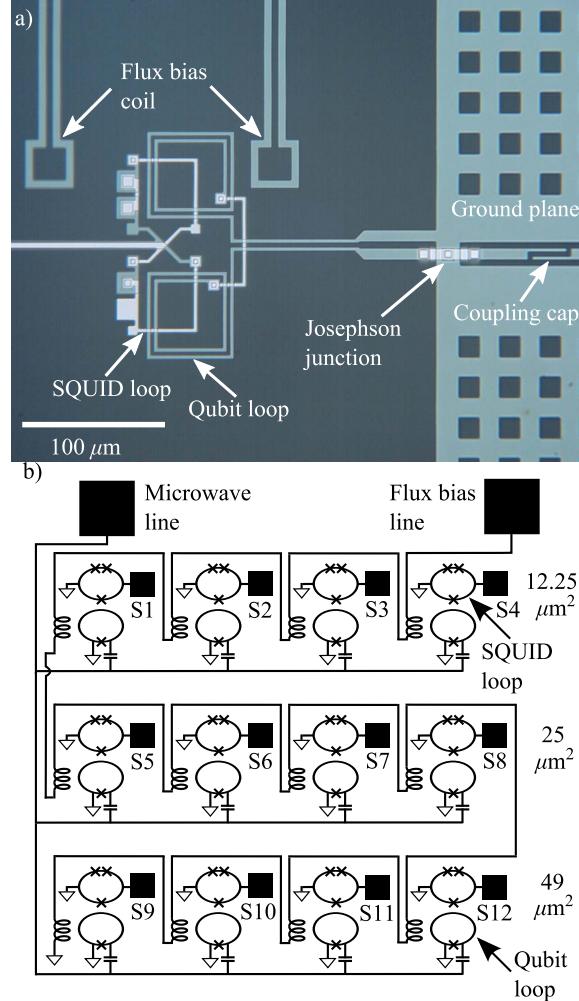


Figure 1. Optical and schematic views of the qubit circuit. (a) Micrograph of an individual qubit circuit consisting of a Josephson junction in a gradiometer loop, state readout measurement SQUID and gradiometric flux bias coil. The perforated ground plane and microwave coupling capacitor are visible at right. (b) Schematic drawing of the full 12-qubit circuit with qubit junction areas listed at right. Microwave lines and flux bias lines are common to all twelve qubit circuits, while SQUID bias lines S1-S12 are individually biased for each circuit.

To accommodate the variation in  $I_c$  by 1  $\mu$ A to 5  $\mu$ A from one deposition to the next, we utilize circuits designed to operate with different target critical current densities. This is accomplished by varying the qubit junction area: 12.25  $\mu\text{m}^2$ , 25  $\mu\text{m}^2$  and 49  $\mu\text{m}^2$  so that we have four qubit circuits of each size on a single die. We deliberately use junctions of large area so that we can obtain meaningful statistics on TLS density of advanced tunnel barrier materials. The respective circuits are designed with a target  $I_c = 1.6 \mu\text{A}$ . The area of the small SQUID junction matches the qubit junction area, and the larger SQUID junctions are scaled by a factor of 1.7. Assuming that  $J_c$  is uniform over the entire die, only four circuits of one particular size will have the proper  $I_c$  on a given die (e.g., four 25  $\mu\text{m}^2$  size circuits are operable, but 12.25  $\mu\text{m}^2$  and 49  $\mu\text{m}^2$  sized circuits have  $I_c$  outside the desired range).

To accommodate the large number of qubit circuits per die, we utilize capacitively coupled microwave lines ( $C = 0.5 \text{ fF}$ ) and inductively coupled flux bias lines common to all twelve qubit circuits. The flux bias lines are connected in series to each separate qubit circuit, as shown in figure 1(b). During

normal operation, all twelve qubits are subjected to flux bias and microwave radiation on the common lines, but the SQUID bias lines are individually controlled for state readout of only one qubit at a time.

The actual qubit junctions are inaccessible for direct measurements of critical current because they are shunted by the qubit inductive loop. For measurement of critical current, we placed eight isolated test junctions with wiring suitable for four-probe measurements around the perimeter of the die. After fabrication, we perform room temperature four-probe measurements of the normal state resistance  $R_n$  of the junctions as an initial screening test for critical current using the Ambegaokar-Baratoff formula [15]

$$I_c = \frac{\pi}{2eR_n} \Delta(T) \tanh\left(\frac{\Delta(T)}{k_B T}\right),$$

where  $e$  is the electron charge,  $T$  is temperature,  $\Delta$  is the superconducting energy gap and  $k_B$  is Boltzmann's constant.

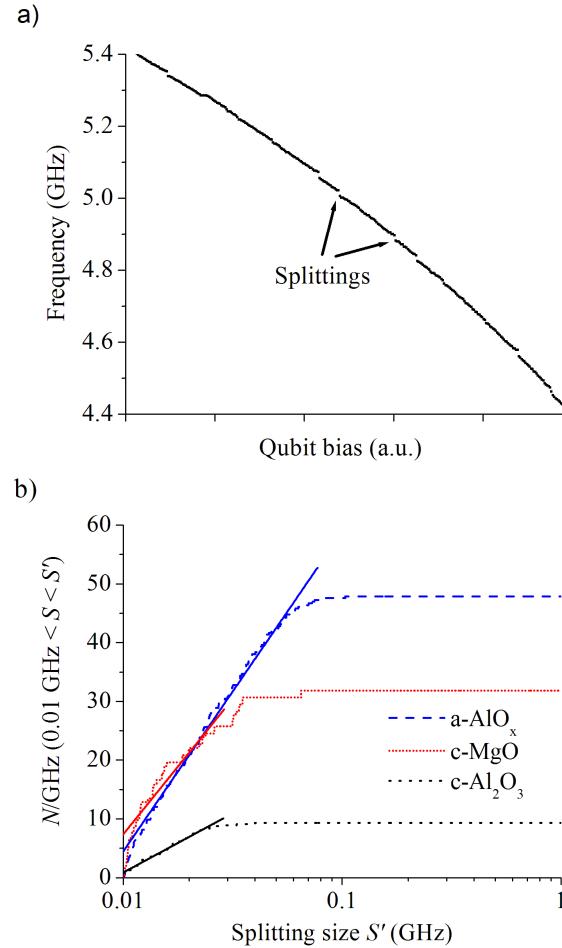


Figure 2. Measurement of the qubit-TLS interaction. (a) Spectroscopy of the  $|0\rangle \rightarrow |1\rangle$  qubit transition as a function of qubit bias for the  $c\text{-Al}_2\text{O}_3$  qubit. (b) Size distribution of the TLS in  $49 \mu\text{m}^2$  junctions normalized to a 1 GHz bandwidth. Based on the slope of the fitted solid lines,  $\sigma h$ , the materials constant describing the TLS defect density is 0.2, 0.4 and  $0.5 (\mu\text{m}^2\text{GHz})^{-1}$  for the  $c\text{-Al}_2\text{O}_3$ ,  $c\text{-MgO}$  and  $a\text{-AlO}_x$  tunnel barriers, respectively.

#### 4. Low Temperature Measurements

We first perform low temperature ( $T = 75$  mK) measurements of the SQUIDs in an adiabatic demagnetization refrigerator (ADR), which requires considerably fewer operational resources than does a dilution refrigerator. We measure SQUID IV curves and SQUID-qubit switching curves in the ADR to

check for proper operation of the SQUID and critical current of the qubit junction. Next we cool the die in a dilution refrigerator ( $T = 20$  mK) where microwave lines are available.

We plot the peak value of the occupation probability of the qubit  $|1\rangle$  state in figure 2(a) as a function of excitation frequency and qubit bias. Along with the expected bias dependence, we find anomalous avoided two level crossings (splittings) in the spectroscopy that result from the qubit resonating with individual TLS in the tunnel barrier [2]. A comparison of the splitting distribution between qubits with amorphous  $\text{AlO}_x$  (a- $\text{AlO}_x$ , data averaged over seven samples), crystalline  $\text{Al}_2\text{O}_3$  (c- $\text{Al}_2\text{O}_3$ , data averaged over three samples) and crystalline  $\text{MgO}$  (c- $\text{MgO}$ , data averaged over two samples) tunnel barriers is shown in figure 2(b). The initial sloped portion of the curves can be approximated by the relation<sup>3</sup>

$$\frac{dN}{dE}(S') - \frac{dN}{dE}(0.01) \approx 2.30\sigma A[\log S' + 2],$$

where  $\frac{dN}{dE}$  is the integrated density of splittings with size  $S/h$  between 0.01 GHz and  $S'/h$ ,  $h$  is

Planck's constant and  $\sigma$  is a materials constant describing the TLS defect density [3]. We assume that any splittings smaller than the arbitrarily assigned 0.01 GHz cutoff frequency are artifacts. However, the choice of cutoff frequency does not affect the slope of the curves,  $2.30\sigma A$ .

As summarized in table 1, we find that  $\sigma$  of the crystalline  $\text{Al}_2\text{O}_3$  tunnel barrier is one third as large as the amorphous  $\text{AlO}_x$  barrier. This corresponds to a 60% reduction in the TLS density and agrees reasonably well with the 80% reduction of [4] obtained from counting the number of TLS in the spectroscopy data. Comparisons between  $\sigma$  are more accurate than comparisons between the number of splittings, which depends on the choice of cutoff frequency.

The crystalline  $\text{MgO}$  qubit had only a slight reduction in  $\sigma$  compared to that of the amorphous  $\text{AlO}_x$  qubit. We attribute this to the large lattice mismatch (8%) between the Re base electrode and  $\text{MgO}$  tunnel barrier, resulting in a large density of defect sites and hence TLS.

Measurement of the energy relaxation time of the  $|1\rangle$  state to the ground state for the  $49\ \mu\text{m}^2$  crystalline  $\text{Al}_2\text{O}_3$  qubit yielded 500 ns. The measurement fidelity is  $\sim 80\%$  and dephasing time  $T_2 \sim 140$  ns, extracted from Rabi oscillations shown in figure 3. These values are comparable to the results obtained from the smaller  $13\ \mu\text{m}^2$  amorphous  $\text{AlO}_x$  qubit fabricated with  $\text{SiN}_x$  insulator [3], which has  $10\times$  lower loss tangent than  $\text{SiO}_2$ . This indicates that a small area ( $13\ \mu\text{m}^2$ ) crystalline  $\text{Al}_2\text{O}_3$  qubit would have improved energy relaxation time and measurement fidelity due to the decreased number of TLS that are expected.

The energy relaxation time of the crystalline  $\text{MgO}$  qubit is significantly shorter than that for a- $\text{AlO}_x$  and c- $\text{Al}_2\text{O}_3$ , as shown in table 1. TLS density  $\sigma$  is similar for  $\text{MgO}$  and  $\text{AlO}_x$ , so the  $\text{MgO}$  qubit should have had a comparable  $T_1$  if dielectric loss were the only loss mechanism present. The short  $T_1$  of the  $\text{MgO}$  qubit may be due to phonon radiation in the tunnel barrier [16]. This is supported by the fact that  $\text{MgO}$  has piezoelectric constants similar to those of  $\text{AlN}$  which was shown to have a short  $\sim 20$  ns energy relaxation time when used as a tunnel barrier material [17].

<sup>3</sup>This equation was derived by neglecting the square-root term in equation (4) of [3], integrating with respect to  $S$  and evaluating from the limits 0.01 GHz to  $S'$ .

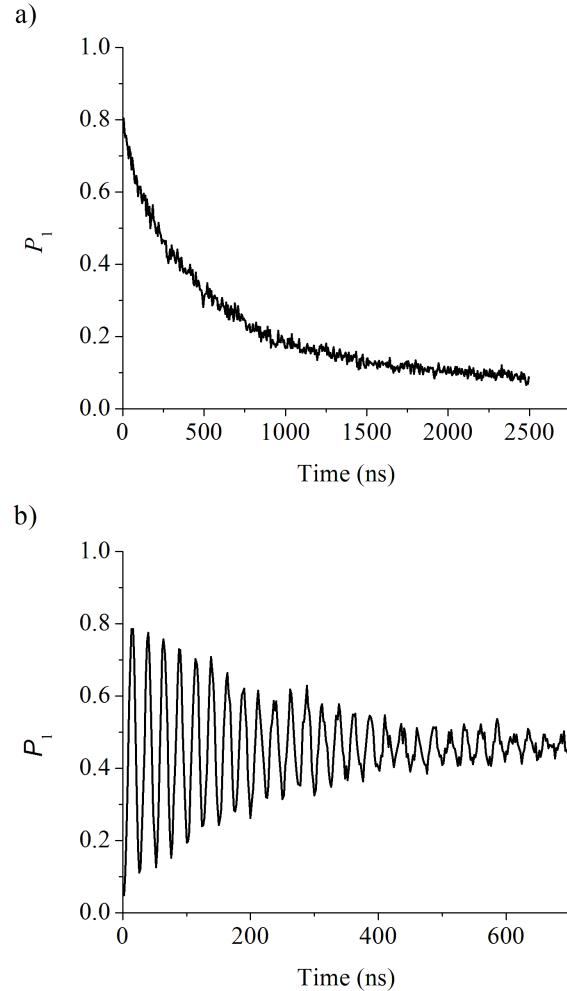


Figure 3. Low temperature ( $T = 20$  mK) measurements for the qubit with c-Al<sub>2</sub>O<sub>3</sub> tunnel barrier. (a) Energy relaxation time  $T_1 = 500$  ns. Measurement fidelity = 80%. (b) Rabi oscillations: dephasing time  $T_2 \sim 140$  ns. Rabi visibility = 70%.

Table 1. Qubit performance comparison between three different Josephson phase qubits. The loss tangent  $\tan \delta$  of the tunnel barrier and cross-over insulator (measured at single photon energy), defect density  $\sigma$  and qubit area  $A$  all affect the measured energy relaxation time  $T_1$ .

Tunnel Barrier			Cross-over Insulator		Qubit	
Material	$\tan \delta$	$\sigma h$ ( $\mu\text{m}^2\text{GHz}^{-1}$ )	Material	$\tan \delta$	$A$ ( $\mu\text{m}^2$ )	$T_1$ (ns)
a-AlO <sub>x</sub>	$10^{-3}$ [3]	0.5	SiN <sub>x</sub>	$10^{-4}$ [11]	13	500 [3]
c-MgO	$10^{-3}$ [11]	0.4	SiO <sub>2</sub>	$10^{-3}$ [11]	25	80
c-Al <sub>2</sub> O <sub>3</sub>	$10^{-5}$ [11]	0.2	SiO <sub>2</sub>	$10^{-3}$ [11]	49	500

## 5. Conclusions

We have presented a Josephson junction phase qubit circuit design that accommodates a variation in critical current density by a factor of five from one deposition run to the next. This design proved to be useful in the early investigation of advanced tunnel barrier materials for quantum computation applications where process control of the junction critical current density has not yet been optimized. Using the new circuit design, we compared the performance of Josephson phase qubits fabricated with MgO and Al<sub>2</sub>O<sub>3</sub> advanced crystalline tunnel barriers to that of AlO<sub>x</sub> amorphous tunnel barrier qubits.

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